IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Eiji Nishibe et al. Art Unit : 2826
Serial No. : 10/007,384 Examiner : Tan N. Tran
Filed : October 22, 2001
Title : SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

DECLARATION OF EIJI NISHIBE UNDER 37 C.F.R. 1.132

I, Eiji NISHIBE declare as follows:

1. I am currently employed by Sanyo Electric Co., Ltd, the assignee of the present application, in the Semiconductor Company LSI Business Unit. Device Engineering Department, 2, Senior staff. I have worked for the assignee for nine (9) years. I have approximately twelve (12) years of experience in semiconductor device fabrication processes. I was educated at Tokyo University of Science, and have earned the Master of Material Science and Technology

2. In preparing this declaration, I have reviewed the Office Action mailed September 30, 2003, as well as the patent specification for the application identified above including the pending claims. I also have reviewed the cited reference, U.S. Patent No. 5,286,995 to Malhi.

3. It is my opinion for the reasons expressed below that the process disclosed in the cited reference does not result in a structure having a first gate insulating film that does not extend lower than the second gate insulating film, as recited in claim 1.

4. Attached to this declaration are the following Exhibits:

Exhibit 1 is FIG. 1 of the Malhi patent.

Exhibit 2 illustrates the resulting structure of the reference when process according to the specification.

Exhibit 3 is chart of the conventional Local Oxidation of Silicon (LOCOS) process.

Exhibit 4 illustrates the thermal oxidation step of the LOCOS process of the reference resulting in a first gate insulating film 28b lower than a second gate insulating film.

5. The Office Action alleges that the Malhi patent discloses a first gate insulating film that does not extend lower than a second gate insulating film. Referring to attached Exhibit 1 (equivalent to FIG. 1 of Malhi), it is alleged that layers 28b, 28c (corresponding to the first gate insulating film), and layer 28a (corresponding to the second gate insulating layer) are represented as "wherein the first gate insulating film does not extend lower than the second gate insulating film."

6. In actuality, the process disclosed by the Malhi patent would result in a structure with layers 28b, 28c that do extend lower than layer 28a because layers 28b, 28c are formed by a conventional LOCOS (local oxidation of silicon) field oxidation process. *See, for example*, col. 2, line 66 to col. 3, line 5.

7. Layers 28b, 28c are formed by the conventional LOCOS field oxidation process that a person of ordinary skill in the art would understand includes: (1) formation of a Si_3N_4 on the substrate as a mask, which is characterized by a speed of thermal oxidation that is slower than SiO_2, (2) thermal oxidation carried out so as to form selected thermal oxidation films, and (3) removal of the Si_3N_4. As described below, that process will result in the structure illustrated in Exhibit 2 where layers 28b, 28c do extend below layer 28a.

8. The conventional LOCOS process is represented in Exhibit 3. When the thermal oxidation is carried out where an opening in the Si3N4 layer exists on the substrate, the formed oxidation film extends below the Si3N4 layer as illustrated.

9. Referring to Exhibit 4, as described col. 2 line 66, to col. 3, line 5, (1) a masked Si3N4 layer is formed on the wafer and a thick SiO2 (corresponding to 28b) is formed over the unmasked areas by Si3N4, (2) the Si3N4 is removed with a wet etch from over the wafer surface, and (3) a thin gate oxide, corresponding to layer 28a, is formed on the wafer surface. As a result, the layer 28b extends below the layer 28a. Thus, the first gate insulating layer 28b will extend lower than the second gate insulating layer 28a.

10. In contrast, the process of the present application as recited in claim 1 differs from the conventional manufacturing method for forming the first gate insulating film. The recited process has a feature that an insulating film is formed on the entire surface of the substrate, and the first gate insulating film is patterned in the desired shape so as to form the first gate insulating film.

11. As a result, in the present application the first gate insulating film is not formed at a position lower than the surface position of the substrate, and the first gate insulating film does not extend lower than the second gate insulating film.

12. In view of the above considerations, it is my opinion that the process disclosed in Malhi will not result in the claimed structure of the present application. In particular, the Malhi patent will result in a structure as illustrated in FIG. 9, which is the prior art.

13. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the above-identified application or any patents issued thereon.

Signature: Eiji Nishibe Date: January 21, 2004

Typed/Printed Name : Eiji Nishibe

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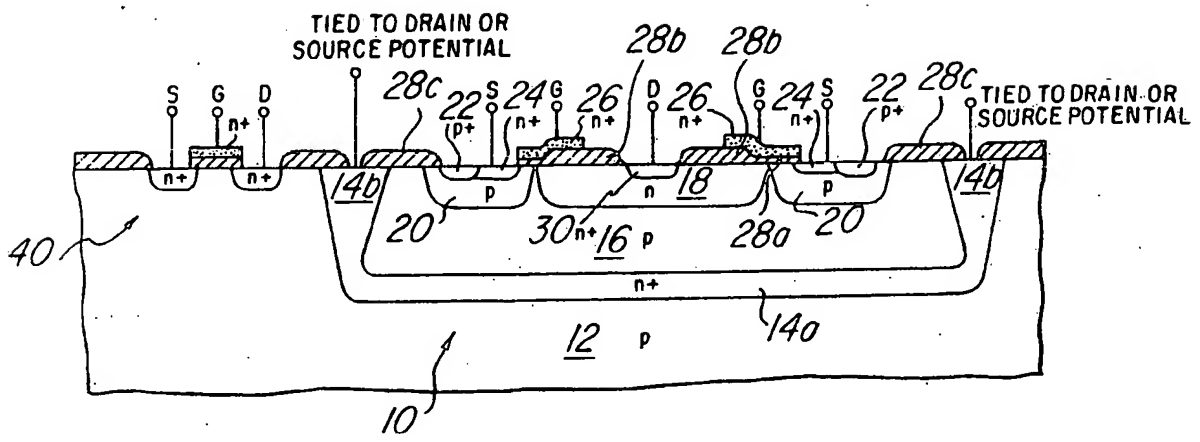

Exhibit 1

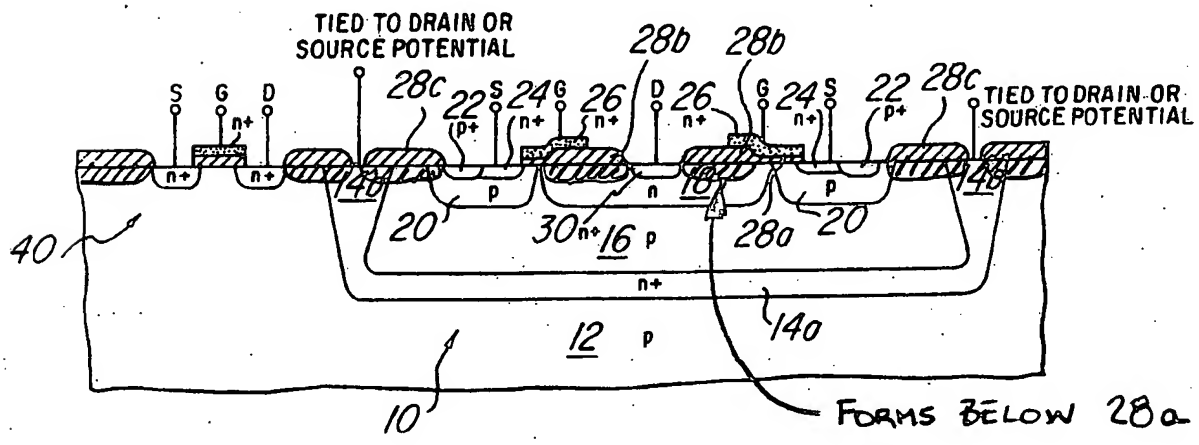

Exhibit 2

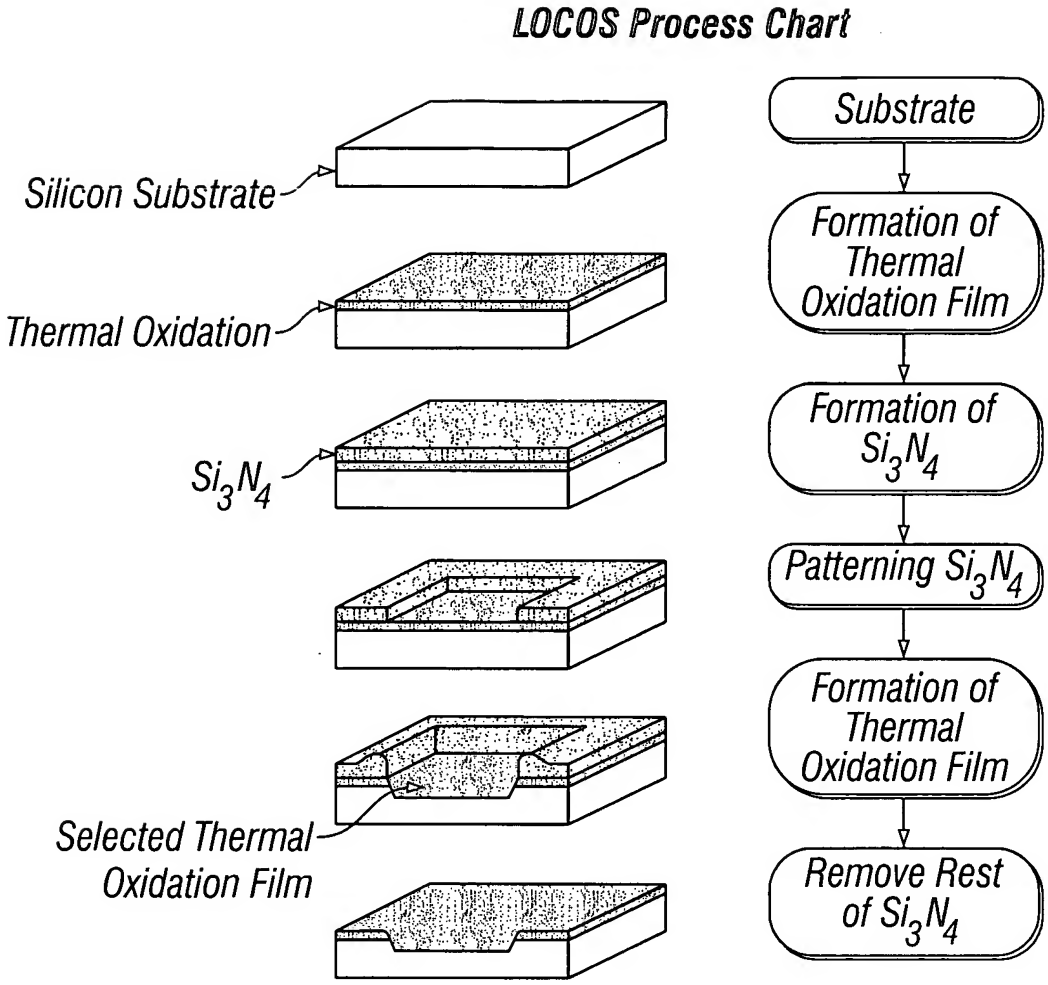

Exhibit 3

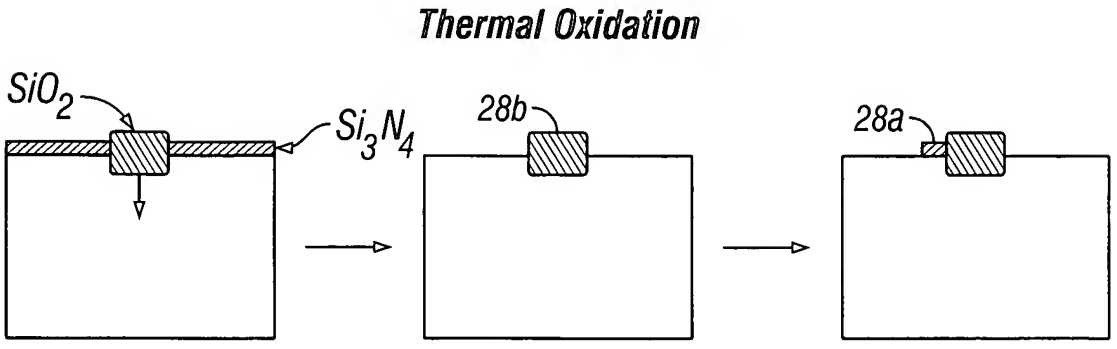

Exhibit 4